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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,951	11/14/2003	Abiola Awujoola	03-1025	6949

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EXAMINER	
WHITMORE, STACY	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,951	AWUJOOLA ET AL.	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2006*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-16 and 18-25* is/are rejected.

7)☒ Claim(s) *3-4, 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL ACTION

Claim Objections

1. Claim 25 is objected to because of the following informalities: Claim 25 includes "110 counts", and apparently should be I/O counts. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 5-8,12-15, and 19-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Shrauger (US Patent Application Publication 2002/0145185).

3. As for the claims Shrauger discloses the invention as claimed, including:

1. An apparatus for packaging and providing backside access to an integrated circuit, the apparatus comprising:
a carrier substrate [fig. 1, element 1.];
an array of package connection pads positioned around a periphery of a top surface of the carrier substrate [fig. 1, element 7];
a ring of die connection pads positioned within the array of package connection pads, the ring of die connection pads configured to provide electrically connectivity to an integrated circuit die by removal of as much as all of the access region without damaging electrical integrity of any circuit traces of the carrier substrate [fig. 1, element 3, paragraph 0034];

2. The apparatus of claim 1, wherein the carrier substrate comprises a plurality of circuit traces configured to electrically connect the array of package connection pads to the ring of die connection pads without penetrating the access region [paragraph 0034, PGA or BGA, fig. 7];

5. The apparatus of claim 1, wherein the carrier substrate comprises a single signal layer [fig. 7, paragraph 0034];

6. The apparatus of claim 1, wherein the access region corresponds to a substrate cavity [paragraph 0034];

7. The apparatus of claim 6, wherein the integrated circuit die is positioned within the substrate cavity [fig. 7, paragraph 0034];

8. The apparatus of claim 7, further comprising a package body molded over the integrated circuit die [fig. 7, paragraph 0034];

12. The apparatus of claim 1, further comprising an array of solder balls attached to the array of package connection pads [fig. 7 showing solder balls connecting the MEMS, paragraph 0035];.

13. The apparatus of claim 1, wherein the carrier substrate is a printed circuit board [paragraph 0037];

14. The apparatus of claim 1, wherein the array of package connection pads is configured to receive an array of solder balls [paragraph 0035];

15. A method for designing an integrated circuit carrier to an integrated circuit, the method comprising:

placing an array of package connection pads around a periphery of a top surface of a carrier substrate [fig. 1, element 7];

placing a ring of die connection pads within the array of package connection pads, the ring of die connection pads configured to provide electrically connectivity to an integrated circuit die, reserving an access region for conducting backside access to the IC die, wherein no signal traces are disposed [fig. 1, element 3, paragraph 0034];

19. The method of claim 15, further comprising routing a plurality of traces between a ring of die connection pads and an array of package connection pads without penetrating the access region [paragraph 0034, fig. 6 and 7];

20. A method for packaging and providing access to an integrated circuit, the method comprising:
electrically connecting an integrated circuit die to a ring of die connection pads on a top surface of a carrier substrate [fig. 1, connection of elements 3 to 7];
attaching a cover to a bottom surface of the carrier substrate [figs. 6-7, paragraphs 0034-0035];
removing a portion of the cover within an access region in order to access a backside of the IC without damaging any electrical connectivity of the substrate [paragraph 0034];
21. The method of claim 20, further comprising placing the integrated circuit die within a cavity of the carrier substrate [fig. 7, paragraph 0034];
22. The method of claim 20, further comprising molding a package body over the integrated circuit die [fig. 7];
23. The method of claim 20, further comprising attaching an array of solder balls to the array of package connection pads [paragraph 0035];
24. A system for packaging and providing backside access to a wide variety of integrated circuits, the system comprising:
a plurality circuit carriers, each circuit carrier configured to receive a range of integrated circuit sizes and I/0 counts, each circuit carrier overlapping in size range with at least one other circuit carrier of the plurality of circuit carriers [paragraphs 0004-0008 – showing that multiple dies and substrates can be used as well as various sizes of dies and therefore different interconnections such as I/O or connections to the substrate, each circuit carrier comprising:
a carrier substrate [fig. 1, element 1];
an array of package connection pads positioned around a periphery of a top surface of the carrier substrate [fig. 1, element 7];
a line of die connection pads positioned within the array of package connection pads [fig. 1, element 3];
an access region positioned with the ring of die connection pads, the access region configured to facilitate backside access to the IC die by removal of as much as all of the

access region without damaging electrical integrity of any circuit traces of the carrier substrate [fig. 6-7, paragraph 0034];

25. The system of claim 24, wherein each circuit carrier overlaps in size range with no more than two other circuit carriers of the plurality of circuit carriers [fig. 1, paragraphs 0004-0008];

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 10, 11, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shrauger (US Patent Application Publication 2002/0145185) in view of Le Coz (US Patent Application Publication 2001/0039644).

5. As for claims 10-11, 16 and 18, Shrauger discloses the invention substantially as claimed including the apparatus and method for designing the IC carrier with backside access as rejected in claims 1 and 15 above.

Shrauger does not specifically disclose a ground ring surrounding the access region; wherein the ring of die connection pads comprises a quadrant of bonding fingers that are substantially equally distanced from an edge of the integrated circuit die;

Le Coz discloses a ground ring surrounding an [paragraphs 0038, 0058, 0078, and 0082, page 20, right hand side]; wherein the ring of die connection pads comprises a quadrant of bonding fingers that are substantially equally distanced from an edge of the integrated circuit die [fig. 2A]; selecting a quadrant shape for a quadrant of bonding fingers such that the bonding fingers are substantially equally distanced to an edge of an integrated circuit die [fig. 2A, paragraphs 0013, 0028-0029, 0077,-0078, 0081-0082, 0093-0094, Table 0021];

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Shrauger and Le Coz because having a ground ring as well as signal and voltage rings allow for correct voltages to be supplied to chip devices and therefore for the proper operation of the chip, and further having a quadrant of bonding pad fingers equally distanced from the edge of the IC die, and having a shape for a quadrant of bonding fingers substantially equally distanced to an edge of the IC die would reduce signal skew to the IC, thereby improving circuit operation.

6. Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shrauger (US Patent Application Publication 2002/0145185) in view of Chao (US Patent Application Publication 2002/0053731).

7. As for claim 9, Shrauger discloses the invention substantially as claimed, including the apparatus for packaging and providing backside access as cited above in the rejection of claim 1.

Shrauger does not specifically disclose a heat spreader thermally connected to

a bottom surface of the substrate.

Chao discloses a heat spreader thermally connected to a bottom surface of the substrate [abstract, paragraphs 0028, 0030 and 0031].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Shrauger and Chao because using a heat spreader as does Chao, would provide a means for creating a cavity in a alternate way, thereby improving versatility and would also improve mounting ability for the substrate, thereby improving access to the circuits

8. Claims 3-4, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to disclose either singularly or in combination the invention as claimed, including wherein the array of package connection pads has a perimeter depth substantially equal to a maximum number of signal traces routable between minimally spaced package connection pads; wherein the array of package connection pads has a perimeter depth that is less than a package connection pad spacing divided by a trace pitch; and selecting a perimeter depth for the array of package connection pads that is less than an package connection pad spacing divided by a trace pitch.

10. Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571)

272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stacy A Whitmore
Primary Examiner
Art Unit 2825

SAW
August 6, 2006